CBCS Scheme

USN | | | | | | | | | | |

15CS34

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. With a neat diagram, explain basic operational concept of computer. **(06 Marks)**
b. What is performance measurement? Explain overall SPEC rating for computer. **(04 Marks)**
c. Draw single bus structure, discuss about memory mapped I/O. **(06 Marks)**

OR

2 a. What is an addressing mode? Explain any three addressing modes with example. **(10 Marks)**
b. Explain BIG-ENDIAN and LITTLE-ENDIAN methods of byte addressing with proper example. **(06 Marks)**

Module-2

3 a. What is an Interrupt? With example illustrate concept of interrupt. **(06 Marks)**
b. Define Exception. Explain 2 kinds of exception. **(04 Marks)**
c. With a neat diagram explain DMA controller. **(06 Marks)**

OR

4 a. Explain PCI bus. **(05 Marks)**
b. List SCSI bus signal with their functionalities. **(05 Marks)**
c. Explain the tree structure of USB with split bus operation. **(06 Marks)**

Module-3

5 a. Briefly explain any two mapping function used in cache memory. **(08 Marks)**
b. With a neat diagram explain the internal organization of memory chip (2M×8 and dynamic memory chip). **(08 Marks)**

OR

6 a. Explain the following :
i) Hit Rate and Miss penalty ii) Virtual memory organization. **(08 Marks)**
b. With diagram explain how virtual memory translation take place. **(08 Marks)**

Module-4

7 a. Draw 4-bit carry-look ahead adder and explain. **(06 Marks)**
b. Perform multiplication for -13 and +09 using Booth's Algorithm. **(06 Marks)**
c. Design a logic circuit to perform addition/subtraction of 'n' bit number X and Y. **(04 Marks)**

OR

8 a. Explain IEEE standard for floating point number. **(06 Marks)**
b. With figure explain circuit arrangement for binary division. **(10 Marks)**

Module-5

9 a. With a figure explain single bus organization of datapath inside a processor. **(08 Marks)**
b. What are the actions required to Execute a complete instruction Add (R3), R_1. **(02 Marks)**
c. Give the control sequence for execution of instruction ADD (R3), R_1. **(06 Marks)**

OR

10 a. Briefly explain the block diagram of camera. **(08 Marks)**
b. Explain multiprocessors. Justify how time is reduced. **(08 Marks)**

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